An n-channel MOSFET MI, has its gate coupled its drain. The drain of Ml and the gate of MI are coupled to the supply voltage level Vcc. An n-channel MOSFET M2, has its gate coupled to its drain. The gate and drain of M2 are coupled to the source of MI. An n-channel MOSFET M3, has its gate coupled to its drain. The gate of M3 and the drain of M3 are coupled to the source of M2. An n-channel MOSFET M41 has its drain coupled to the drain of M3. The source of M4 is coupled to the source of M3. The gate of M4 is coupled to be controlled by a control voltage level ENl. An n-channel MOSFET M5, has its gate coupled to the gate of M3. The drain of M5 is coupled to the source of M3. The source of M5 is coupled to a substrate node Vbb. An n-channel MOSFET M6, has its drain coupled to the drain of M5. The source of M6 is coupled to the source of M5 and to the substrate node Vbb. The gate of M6 is coupled to be controlled by a control voltage level EN2. The substrate node Vbb, is coupled to the substrate of a integrated circuit chip on which the substrate voltage regulator circuit is contained.

Applicant respectfully submits that no new matter has been added as a result of the proposed amendment to the specification.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 19-20. The specific amendments to individual claims are detailed in the following marked up set of claims.

19. (Amended) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on an integrated circuit substrate; and

a substrate voltage regulator circuit coupled to the integrated circuit substrate for setting a substrate voltage bias level[.], including:

a series of diodes coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

Docket No. 303.221US4
WD # 463148

Micron Ref. No. 94-0108

Clean Version of Pending Claims

ON-CHIP SUBSTRATE REGULATOR TEST MODE
Applicant: Gary R. Gilliam
Serial No.: 09/935,232

Claims 19-43, as of November 25, 2002 (date of response to first office action filed).

19. (Amended) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on an integrated circuit substrate; and

a substrate voltage regulator circuit coupled to the integrated circuit substrate for setting a substrate voltage bias level, including:

a series of diodes coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

20. (Amended) The DRAM of claim 19, wherein the substrate voltage regulator circuit comprises:

a series of diode connected transistors coupled between a supply voltage source and the integrated circuit substrate, and at least one bypass transistor coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing the one diode connected transistor.

21. The DRAM of claim 19, wherein each diode of the series of diodes has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diodes of the series of diodes.

22. A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

23. The DRAM of claim 22 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode in the series of diodes for electrically bypassing a plurality of diodes.

24. The DRAM of claim 22 wherein at least one bypass transistor is coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

25. The DRAM of claim 22 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

26. The DRAM of claim 22 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

27. A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

28. The DRAM of claim 27 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

29. The DRAM of claim 27 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

30. A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises a plurality of bypass transistors coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

31. The DRAM of claim 30 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

32. The DRAM of claim 30 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

33. A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

34. The DRAM of claim 33 wherein the at least one bypass transistor is coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

35. The DRAM of claim 33 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

36. The DRAM of claim 33 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

37. A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

38. The DRAM of claim 37 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing a plurality of diode connected transistors.

39. The DRAM of claim 37 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

40. The DRAM of claim 37 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit memory device such that the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.

41. A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and a plurality of bypass transistors coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

42. The DRAM of claim 41 wherein the plurality of bypass transistors is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

43. The DRAM of claim 41 wherein the plurality of bypass transistors is turned on during normal operation of the integrated circuit memory device such that the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.